REMARKS

Claims 1-47 are pending in the present application. Claims 1-3 and 16 have been rejected under § 103 as being unpatentable over Bell (US 5,642,075) (Bell) in view of Blake (US 6,847,904) (Blake). Claims 1-14, 16-27, and 38-47 have been rejected under § 103 as being unpatentable over Lee (US 2003/0152056) (Lee) in view of Lin (US 2004/0038701) (Lin) and Blake. Claims 15 and 28 have been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake, and further in view of Yu et al. (US 5,365,190) (Yu). Claims 29-37 have been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake, and further in view of Gunzelmann et al (US 2004/0097250) (Gunzelmann).

Amended claim 1 recites an RF apparatus formed using an integrated circuit comprising "power amplifier circuitry formed using the integrated circuit, wherein the integrated circuit includes a digital interface for providing an interface between the power amplifier circuitry and an external controller, wherein the interface is a digital interface for receiving a digital signal from the external controller, and wherein the digital signal contains power control data," and "circuitry for generating a power ramp profile to vary the output power of the RF power amplifier based on a desired output power level relating to the digital signal from the external controller."

Bell discloses an amplifier circuit using an automatic gain control (AGC). The circuit of Bell is designed to adjust the gain of amplifier 14 so that the output Vout is maintained at a desired RMS value. Bell uses an analog reference voltage Vref to maintain the RMS value of Vout. Blake discloses an programmable gain amplifier. Blake discloses an external analog reference voltage Vref that is connected to a gain setting resistor ladder network 112. In both Bell and Blake, Vref is not a digital signal, but rather is an analog reference voltage. Also, it appears that Vref is constant, and therefore is not used to vary the output power of an amplifier based on

a desired output power level that relates to a digital signal from an external controller. It is unclear from the Blake reference how Vref could be a digital signal from an external controller, likewise with Bell. The Office Action also states that that the logical circuits in FIGS. 6A and 6B of Bell are digital interfaces. FIGS. 6A and 6B of Bell show the gain latch, ripple counter, delay and reset control circuitry shown in FIG. 1. It is also unclear how these could be interfaces that meet the requirements of amended claim 1.

As mentioned above, claim 1 has also been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake.

Lee discloses a wireless local area network (WLAN) transceiving integrated circuit (IC), including a WLAN interface, an input buffer and controller, and a processor. An IC of Lee (e.g., IC 350 of FIG. 3B) includes a power amplifier 352, core components 351, and serial and parallel interfaces 320 and 324 to interface with a host 322. An IC of Lee (e.g., IC 400 of FIG. 4A) may include a baseband 404. Lee does not teach or suggest, however, an integrated circuit with a digital interface for providing an interface between the power amplifier circuitry and an external controller, wherein the interface is a digital interface for receiving a digital signal from the external controller, and wherein the digital signal contains power control data. The interface between the power amplifier 352 and the core components 351 (FIG. 3B) appears to include an transmit signal TX and an analog power control signal TX_PC. The interfaces 320 and 324 (FIG. 3B) do not provide an interface between the power amplifier 352 and an external controller.

Lin discloses a wireless transmission apparatus used for transmitting an RF signal. Like Lee, Lin also does not teach or suggest an integrated circuit with a digital interface for providing an interface between the power amplifier circuitry and an external controller, wherein the interface is a digital interface for receiving a digital signal from the external controller, and

wherein the digital signal contains power control data. The power amplifier 118 receives an RF input signal R118 and an analog control signal from the power control loop 116.

The Office Action states that Blake discloses a digital interface for controlling a power amplifier. Applicants assert that the analog reference voltage Vref does not meet the requirements of amended claim 1, as is discussed in detail above.

For at least these reasons, applicant asserts that amended claim 1 is allowable over the cited prior art. Since dependent claims 3-17 depend from amended claim 1, it is also believed that these claims are allowable over the prior art.

Amended claim 18 recites a method of amplifying RF signals comprising "providing an RF power amplifier formed on an integrated circuit," "storing a plurality of ramp profiles in the integrated circuit," "receiving one or more digital control signals containing power control data from a controller that is external to the integrated circuit, wherein the control signals are received over a digital interface," and "selecting one of the ramp profiles to vary the output power of the RF power amplifier based on a desired output power level relating to one or more of the digital control signals from the controller."

For at least the reasons set forth above with respect to amended claim 1, applicant asserts that amended claim 18 is allowable over the prior art. Since dependent claims 20-28 depend from amended claim 18, it is also believed that these claims are allowable over the prior art.

Amended claim 38 recites an RF power amplifier module comprising "power amplifier circuitry formed using a first integrated circuit," "control circuitry formed using a second integrated circuit," "a digital interface formed using the first integrated circuit, wherein the digital interface is configured to allow digital power control signals from an external controller to be received by the power amplifier circuitry," and "memory formed using one of the first and second

integrated circuits, wherein a plurality of ramp profiles are stored in the memory for varying the output power of the power amplifier circuitry based on desired output power levels relating to one or more of the digital power control signals."

For at least the reasons set forth above with respect to amended claim 1, applicant asserts that amended claim 38 is allowable over the prior art. Since dependent claims 39-47 depend from amended claim 38, it is also believed that these claims are allowable over the prior art.

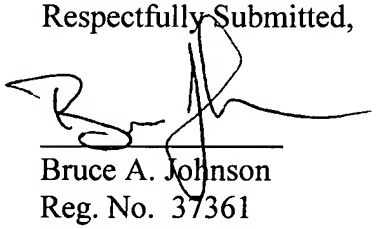
As mentioned above claim 29 has been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake, and further in view of Gunzelmann. Lee, Lin, and Blake are discussed above. Gunzelmann discloses a transmission configuration for a mobile radio communication system. Gunzelmann shows an interface 2 that includes conductors 21, 22, 23, and 24. Conductor 21 carries a digital signal and is designed for transmission of the payload data which is provided from a digital signal processor. The module 3 (including the power amplifier 31) of Gunzelmann does not appear to receive an analog RF input signal to be amplified, but rather appears to receive a digital signal, which is converted into a signal to be amplified.

For at least these reasons, and for reasons set forth above with respect to amended claim 1, applicant asserts that amended claim 29 is allowable over the prior art. Since dependent claims 39-47 depend from amended claim 29, it is also believed that these claims are allowable over the prior art.

It is respectfully submitted that all claims are patentable over the prior art. It is further more respectfully submitted that all other matters have been addressed and remedied and that the application is in form for allowance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Bruce A. Johnson, Applicants' Attorney at 512-301-9900 so that such issues may be resolved as expeditiously as possible.

Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 to deposit account number 50-3864 (Johnson & Associates).

Respectfully Submitted,



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Date

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